.17. (First Amendment) A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second digital signal that varies between the first voltage level and a third voltage level; [and]

a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter[.]; and

a resistive element coupled between said first voltage supply and the gate of said pass gate transistor, the resistive element cooperating with a parasitic capacitor defined by the drain and gate of said pass gate transistor to increase the applied voltage to the gate of said pass gate transistor.

REMARKS

In the Office Action mailed August 2, 1999, claims 1-20 (all claims) are rejected under 35 U.S.C. 103 as obvious in light of any one of Fox, U.S. Patent No. 3,579,023, Nelson, U.S. Patent No. 4,507,618, and GB 1,287,021.

All claims recite a specific application of an electronic circuit configuration for the purpose of converting a binary input signal with a first two levels to a binary output signal with a second two levels. Accepting, for the sake of argument, that the particular circuit structure is "notoriously well known in the art" (to cite the Office Action), the claimed invention is not anticipated unless the prior art teaches the circuit utilized in the particular manner which is claimed.

It would not, as Examiner argues, be obvious to substitute an FET for a resistor to save chip real estate to arrive at the present invention. The FET does more than save chip real estate; the FET has characteristics which the resistor does not. It is these characteristics (e.g. a pumping action of the FET's parasitic capacitance which may be achieved with additional modifications to the circuit topology) which helps enable the circuit's level-shifting function in the claimed application. The present invention advantageously exploits this pumping action specifically to level-shift a binary input signal. In fact, as taught by the specification of the present application, the binary input signal itself may have properties which operate cooperatively with the FET characteristics to facilitate the level-shifting function of the circuit.

The circuits taught in Fox, Nelson, and GB do not teach an application of an FET-based circuit in which a binary signal, applied to an input of the FET, is level-shifted at an output of the FET as a result of the cooperative interaction of a bias resistor and a capacitance of the FET. The cited references merely teach R-C attenuator circuits with analog inputs and analog outputs. There is no obvious motivation to apply R-C attenuator

circuits to binary signals. The claims clearly recite an application involving level shifting of binary signals. The circuits of the cited reference differ in structure, operation, and application from the claimed invention and cannot render it obvious for these reasons.

Having particularly pointed out the distinction between the cited references and the claims, allowance of all claims is respectfully requested. In the alternative, Applicants request entry of the Response to place the application in better condition for appeal.

Dated: 8/23/99

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